Amendments to the Specification:

Please replace the paragraph beginning at page 10, lines 11-16 with the following paragraph:

--Figure 2 illustrates a block diagram of the logic used to perform the course synchronization. This can be performed by an application specific integrated circuit (ASIC), by a microprocessor, or some other processor. As illustrated in figure 2, the apparatus includes delay 10, multipliers 35, summers 40, absolute value squared 15, integral 20, summation 30 and maximum value selector 25. As illustrated, by the blank boxes 60 and 65, the same circuitry or logic may be duplicated.--

Please replace the paragraph beginning at page 11, lines 1-10 with the following paragraph:

--The fine synchronization process (Figure 3) uses one or more preambles stored in a memory, and matches the stored preambles(s) to the transmitted preamble(s). From the starting point determined by the coarse synchronization and traversing forward and/or backward along the data stream, the encountered preambles are compared to the stored preamble by computing a correlation until a complete match is found. Figure 3 illustrates a block diagram of the logic employed to perform this fine synchronization. This too can be realized by an application specific integrated circuit (ASIC), by a microprocessor, or some other processor. As illustrated in figure 3, the apparatus includes even pn codes 50, odd pn codes 45 multipliers 35, integral 20, and maximum value selector 25. As illustrated, by the blank boxes 55, the same circuitry or logic may be duplicated.